

FIG. 4 PRIOR ART

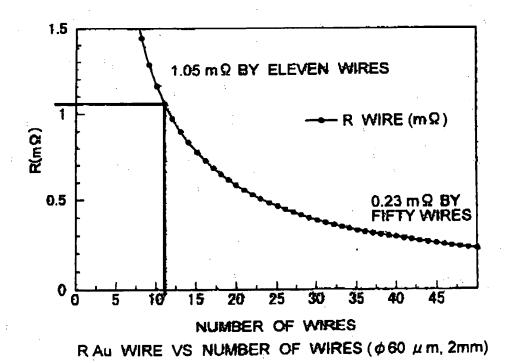
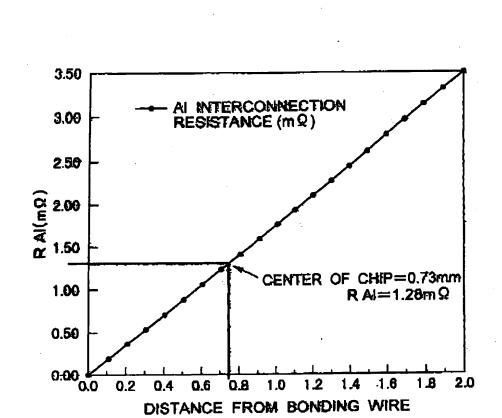


FIG. 5 PRIOR ART





AI INTERCONNECTION RESISTANCE ON SURFACE OF CHIP

FIG. 6 PRIOR ART



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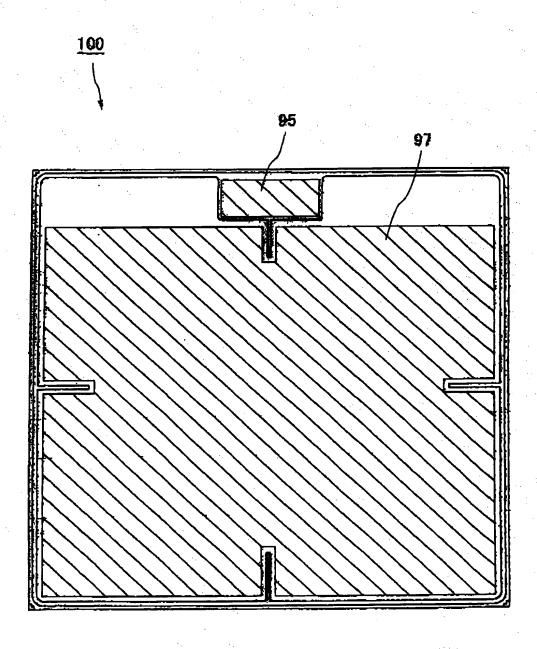


FIG. 8 PRIOR ART



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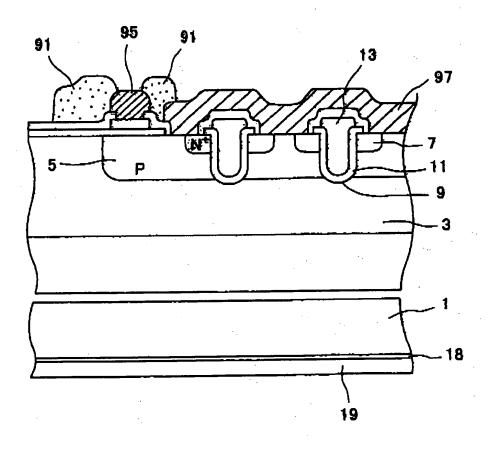


FIG. 7 PRIOR ART



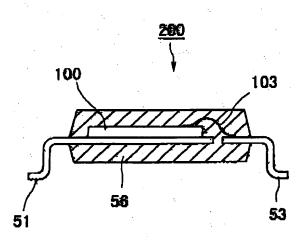


FIG. 9A PRIOR ART

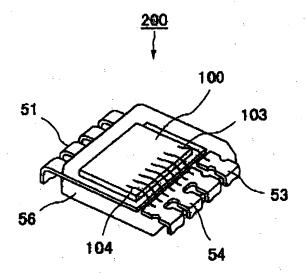


FIG. 9B PRIOR ART



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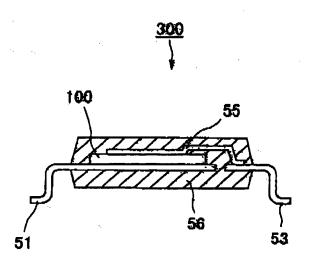


FIG. 10A PRIOR ART

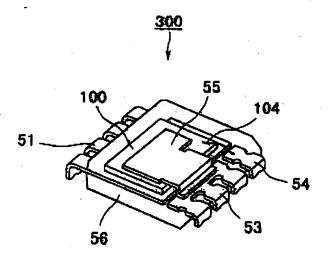


FIG. 10B PRIOR ART